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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ROCHE, TRENTON J	

ART UNIT	PAPER NUMBER
2124	7

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,093	HISATAKE, DERRICK I.	
	Examiner	Art Unit	
	Trent J Roche	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-15,17-22 and 24-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-15,17-22 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to Amendment A filed 12 February 2004.

2. Per applicant's request, amended claims 1, 2, 9, 18 and 25 have been entered. Claims 7, 16, 23 and 30 have been canceled. Claims 1-6, 8-15, 17-22 and 24-29 are pending.

3. Claims 1-30 have been examined.

Drawings

4. The objection to the drawings stated in Paper Num. 5 is hereby withdrawn.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 9-15, 18-22 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,055,632 to Deegan et al in view of U.S. Patent 5,504,801 to Moser et al.

Regarding claim 1:

Deegan et al teach:

- a method comprising sending an upgrade package over a computer network ("transferring the firmware to the non-volatile memory of the programmable controller system by way of the remote network connection." in col. 3 lines 3-5)

- receiving the upgrade package in a network device ("receiving the firmware upgrade at a communication daughterboard of the programmable controller system..." in col. 3 lines 22-24)
- automatically upgrading internal software of a peripheral device installed in the network device using the upgrade package ("the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade." in col. 6 lines 24-28)
- software for upgrading the peripheral device ("a firmware upgrade" in col. 3 lines 20-21)

substantially as claimed. Deegan et al do not explicitly disclose a flash erase file for erasing contents of memory in the peripheral device. Moser et al disclose in an analogous firmware upgrading system the use of a program for erasing contents of memory in the peripheral device as claimed ("With flash memory, programming a memory bank involves first erasing the entire bank..." in col. 4 lines 51-53. A program file for erasing the memory is inherently present.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing technique of Moser et al with the firmware upgrading system of Deegan et al, as this would be one of the "conventional non-volatile memory programming techniques" which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claim 2:

The rejection of claim 1 is incorporated, and further, Deegan et al teach recognizing the received package as an upgrade based on information contained in the upgrade package ("the processor module must eventually...enter the special firmware upgrade mode..." in col. 7 lines 9-10. The fact

that the system enters an upgrade mode means that the system has inherently recognized that the downloaded program is an upgrade, based on the contents of the file.)

Regarding claim 3:

The rejection of claim 1 is incorporated, and further, Deegan et al teach recognizing the received package as an upgrade package based on a filename extension associated with the package (Note rejection regarding claim 2. For the system to enter an upgrade mode, it must recognize the file as an upgrade, therefore inherently recognizes the file by checking the filename.)

Regarding claim 4:

The rejection of claim 1 is incorporated, and further, Deegan et al teach upgrading the internal software as claimed ("the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade." in col. 6 lines 24-28.)

Regarding claim 5:

The rejection of claim 4 is incorporated, and further, Deegan et al teach upgrading the peripheral device as claimed ("enter the special firmware upgrade mode..." in col. 7 line 10. Further, the contents of the upgrade package are parsed into a format suitable for the device, as shown in col. 8 lines 22-36)

Regarding claim 6:

The rejection of claim 5 is incorporated, and further, Deegan et al teach issuing a command to the peripheral device as claimed ("enter the special firmware upgrade mode..." in col. 7 line 10. For the system to have entered an upgrade mode, it must have inherently received a command from the host computer notifying the device of an available upgrade.)

Regarding claim 9:

Deegan et al teach:

- a system comprising a computer network, a network device coupled to the network, a peripheral device installed within the network device; wherein the network device comprises a processor configured to receive an upgrade package as claimed (Note Fig. 1 and 2)
- software for upgrading the peripheral device ("a firmware upgrade" in col. 3 lines 20-21)

substantially as claimed. Deegan et al do not explicitly disclose a flash erase file for erasing contents of memory in the peripheral device. Moser et al disclose in an analogous firmware upgrading system the use of a program for erasing contents of memory in the peripheral device as claimed ("With flash memory, programming a memory bank involves first erasing the entire bank..." in col. 4 lines 51-53. A program file for erasing the memory is inherently present.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing technique of Moser et al with the firmware upgrading system of Deegan et al, as this would be one of the "conventional non-volatile memory programming techniques" which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claim 10:

The rejection of claim 9 is incorporated, and further, Deegan et al teach a processor as claimed (Note Fig. 1 item 22, the microprocessor is installed on the remote device, which controls the upgrading of the firmware once it is downloaded to the system.)

Regarding claims 11-13:

The rejection of claim 9 is incorporated, and further, claims 11-13 are rejected for the reasons set forth in connection with claims 2-4, respectively.

Regarding claim 14:

The rejection of claim 13 is incorporated, and further, claim 14 is rejected for the reasons set forth in connection with claim 5.

Regarding claims 15:

The rejection of claim 14 is incorporated, and further, claims 15 is rejected for the reasons set forth in connection with claim 6.

Regarding claim 18:

Deegan et al teach:

- a computer-readable medium that stores computer-executable instructions ("a computer system...and...a plurality of programmable controller modules..." in col. 11 lines 64-66)
- recognize a received package as an upgrade package intended for a peripheral device installed in a network device ("the processor module must eventually...enter the special firmware upgrade mode..." in col. 7 lines 9-10. The fact that the system enters an upgrade mode

means that the system has inherently recognized that the downloaded program is an upgrade.)

- automatically upgrade internal software in the peripheral device using the upgrade package ("the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade." in col. 6 lines 24-28)
- software for upgrading the peripheral device ("a firmware upgrade" in col. 3 lines 20-21)

substantially as claimed. Deegan et al do not explicitly disclose a flash erase file for erasing contents of memory in the peripheral device. Moser et al disclose in an analogous firmware upgrading system the use of a program for erasing contents of memory in the peripheral device as claimed ("With flash memory, programming a memory bank involves first erasing the entire bank..." in col. 4 lines 51-53. A program file for erasing the memory is inherently present.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing technique of Moser et al with the firmware upgrading system of Deegan et al, as this would be one of the "conventional non-volatile memory programming techniques" which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claims 19 and 20:

The rejection of claim 18 is incorporated, and further, claims 19 and 20 are rejected for the reasons set forth in connection with claims 2 and 4, respectively.

Regarding claim 21:

The rejection of claim 20 is incorporated, and further, claim 21 is rejected for the reasons set forth in connection with claim 5.

Regarding claims 22:

The rejection of claim 21 is incorporated, and further, claims 22 is rejected for the reasons set forth in connection with claim 6.

Regarding claim 25:

Deegan et al teach:

- a port for coupling the apparatus to a network, a peripheral device installed in the apparatus, a processor (Note Fig. 1 and the corresponding section of the disclosure)
- the processor is configured to receive an upgrade package through the port and automatically upgrade internal software in the peripheral device using the upgrade package ("the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade." in col. 6 lines 24-28)
- software for upgrading the peripheral device ("a firmware upgrade" in col. 3 lines 20-21)

substantially as claimed. Deegan et al do not explicitly disclose a flash erase file for erasing contents of memory in the peripheral device. Moser et al disclose in an analogous firmware upgrading system the use of a program for erasing contents of memory in the peripheral device as claimed ("With flash memory, programming a memory bank involves first erasing the entire bank..." in col. 4 lines 51-53. A program file for erasing the memory is inherently present.) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing

technique of Moser et al with the firmware upgrading system of Deegan et al, as this would be one of the "conventional non-volatile memory programming techniques" which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claim 26:

The rejection of claim 25 is incorporated, and further, claim 25 is rejected for the reasons set forth in connection with claim 2.

Regarding claim 27:

The rejection of claim 26 is incorporated, and further, claim 27 is rejected for the reasons set forth in connection with claim 3.

Regarding claim 28:

The rejection of claim 25 is incorporated, and further, claim 28 is rejected for the reasons set forth in connection with claim 5.

Regarding claims 29:

The rejection of claim 28 is incorporated, and further, claim 29 is rejected for the reasons set forth in connection with claims 6.

7. Claims 8, 17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,055,632 to Deegan et al, in view of U.S. Patent 5,504,801 to Moser et al, further in view of U.S. Patent 6,601,212 to Guha et al.

Regarding claim 8:

The rejection of claim 1 is incorporated, and further, neither Deegan et al nor Moser et al teach sending a message indicating success or failure of the upgrade as claimed. Guha et al disclose in an analogous firmware upgrading system sending a message indicating success or failure to the client computer ("If an error is found, an error message will be sent to the client computer...if an error is not found, the peripheral device sends a download successful message to the client computer..." in col. 4 lines 16-30). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to implement the message indication capabilities of Guha et al in the firmware upgrading system of Deegan et al modified by Moser et al, implemented via the addition of instructional code to transmit messages, as this would ensure that the upgrade is completed successfully by enabling the host computer to attempt to resend the upgrade if a failed upgrade message is received in the system disclosed by Deegan et al modified by Moser et al.

Regarding claims 17 and 24:

Claims 17 and 24 recite a system and article for performing the method of claim 8, and are rejected for the reasons set forth in connection with claim 8.

Response to Arguments

8. Applicant's arguments filed 12 February 2004 have been fully considered but they are not persuasive.

Per claims 1-6, 9-15, 18-22 and 25-29:

The applicant states that Deegan et al do not suggest or teach the newly added limitation regarding the use of a flash erase file to erase memory locations of a peripheral device, and the use of a flash erase file during an upgrade of a peripheral device. Applicant's arguments with respect to claims 1-6, 9-15, 18-22 and 25-29 have been considered but are moot in view of the new ground(s) of rejection. It is noted that Moser et al discloses the use of a flash erase file during the upgrade of a peripheral device for erasing the memory locations of a peripheral device. Accordingly, the rejections of claims 1-6, 9-15, 18-22 and 25-29 are maintained.

Per claims 8, 17 and 24:

The applicant states that Deegan et al nor Guha et al disclose or suggest the newly added limitation regarding the use of a flash erase file to erase memory to prepare the peripheral device for an upgrade. Furthermore, the applicant fails to show that the reasons to combine and motivations concerning the rejections of claim 8, 17 and 24 are improper. As has been shown above, the rejections of independent claims 1, 9 and 18 are proper, and as such, the argument that claims 8, 17 and 24 are allowable as being dependent on an allowable base claim is considered moot. Therefore, the rejections of claims 8, 17 and 24 are proper and maintained.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the

mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trent J Roche whose telephone number is (703)305-4627. The examiner can normally be reached on Monday - Friday, 9:00 am - 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trent J Roche
Examiner
Art Unit 2124

TJR

TODD INGBERG
PRIMARY EXAMINER